OEM MANUAL

PC-02 HOST ADAPTER

OPERATING AND SERVICE MANUAL NO. 63223-001 Rev. A

FORWARD

This manual provides operating and service information for the PC-02 Host Adapter, Manufactured by Wangtek Incorporated, 41 Moreland Road, Simi Valley, California.

The content includes a detailed product description, specifications, installation and operation instructions. Also included are theory of operation, maintenance and parts replacement instructions.

TECHNICAL SUPPORT

If for any reason you require product technical support, please contact the OEM or Distributor where you first purchased your equipment. If they cannot help you or at their direction, Wangtek Technical Support can be reached at:

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WARNING

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class B computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial or residential environment. This equipment is a Class B digital apparatus which complies with the Radio Interference Regulations, CRC c.1374.

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Section 1 INTRODUCTION

This section contains information about the purpose, physical and functional description and mechanical and electrical specifications of the Wangtek PC-02 Host Adapter Board.

1.1 Purpose of Equipment

The PC-02 Host Adapter is designed to provide an interface between the IBM Personnel Computer (PC) Bus and QIC-02 interface tape drives. The QIC-02 and IBM PC interface signals are described in Section 3. The PC-02 Host Adapter will operate in an IBM PC/XT, PC/AT or compatible computer using the PC-DOS or MS-DOS operating systems. It is compatible with the SCO-Xenix operating system (V2.2 or higher) "TAR" command using the device drivers supplied by SCO, the PICK operating system (PC/AT only) using the device drivers supplied by PICK and the Novell Netware network operating system.

1.2 Physical Description of Equipment

The host adapter requires a half length IBM PC/XT (8 bit) expansion slot in the computer. Figure 1-1 contains the host adapter board outline, mounting dimensions and interface connections.

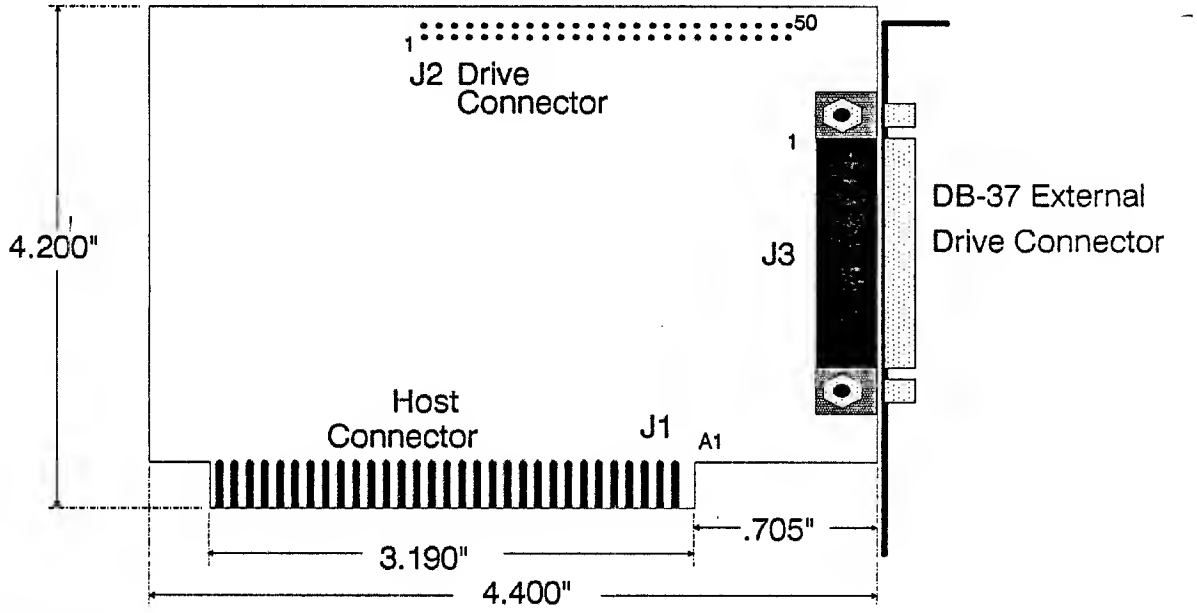


Figure 1-1
PC-02 Host Adapter Mounting and Connections

1.3 Functional Description of Equipment

Operations within the Host Adapter Board are divided into five (5) major functional blocks as outlined in Figure 1-2. The following paragraphs describe the function of each block.

1.4 Host Interface

This block provides the physical interface to the host computer bus. All data, command and status information pass through this block.

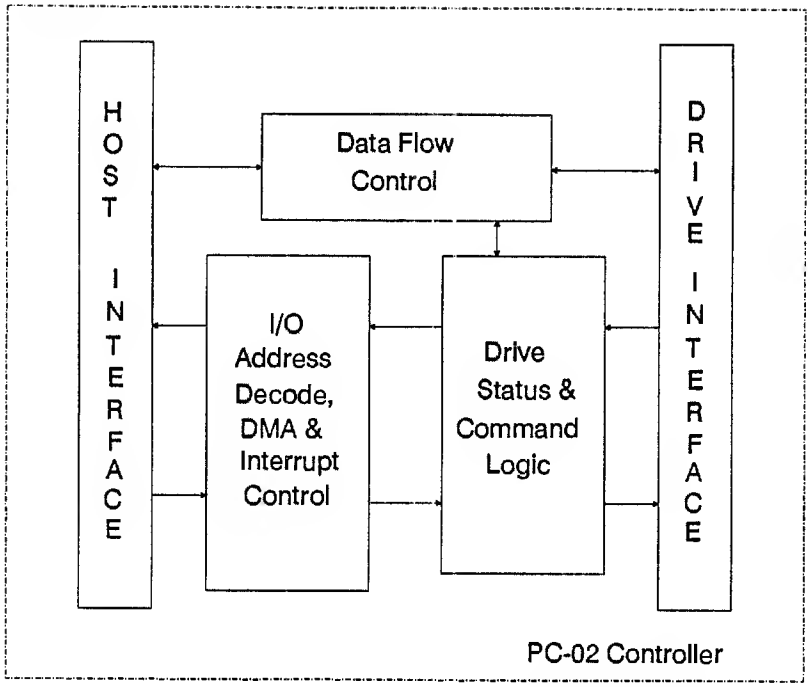


Figure 1-2
PC-02 Controller Functional Block Diagram

1.5 Data Flow Control.

This block is responsible for the flow of data between the host, the PC-02 and the drive. All drive read / write data passes through this block.

1.6 I / O Address, DMA and Interrupt Control

This block is responsible for decoding the PC-02 device I / O Address to enable the adapter for operation. This block is also responsible for the generation of the Interrupt, DACK and DRQ DMA channel signals.

1.7 Drive Command and Status Logic

This block is responsible for communicating commands to the drive and monitoring the drive status during the execution of those commands.

1.8 Tape Drive Interface

The block provides the physical connection to the tape drive. All commands, status and read / write information pass through this block.

1.9 Mechanical and Electrical Specifications

Refer to Table 1-1 for the mechanical and electrical specifications of the PC-02 Host Adapter.

Table 1-1
Mechanical and Electrical Specifications

Host Interface	IBM PC/XT, PC/AT or compatible Technical Reference #6025005, 6936808)
Drive Interface	QIC-02 Intelegent Drive Interface Rev. E
Voltage Requirements	+5 volts ± 5%
Ripple (min./max. must be within 5% supply tollerance)	200mVp-p max.
Current Requirements (assy. #30475)	
+5V	700 mA (nominal)
Power Dissipation	3.5 Watts (nominal)
Current Requirements (assy. #30631)	
+5V	250 mA (nominal)
Power Dissipation	1.3 Watts (nominal)
Temperature	
Operating	5°C to 45°C (40°F to 115°F)
Storage and Shipping	-30°C to 60°C (-22°F to 140°F)
Wet bulb	26°C (78°F) maximum
Humidity	8% to 80% non-condensing
Shock and Vibration	
Non-operational Shock	30 G's, 11mS pulse, 1/2 sine wave
Non-operational Vibration	0 to 63 Hz-.1 inch displacement amplitude (peak to peak) 63 to 500 Hz -1.5 G's
Operational Shock	2.5 G's, 11 mS pulse, 1/2 sine wave
Operational Vibration	0 to 63 Hz-.05 in. displacement amplitude (peak to peak) 63 to 500 Hz-1.0 G's
Altitude	
Operational	-1,000 - 15,000 feet
Non-operational	-1,000 - 50,000 feet
MTBF	>25,000 power on hours
MTTR	<30 minutes average
Dimensions (excluding mounting bracket)	
Height	4.20 inches (106.68mm)
Width	4.40 inches (111.76mm)
Thick	0.550 inches (13.97mm), including Mounting bracket
Weight (board)	0.5 pounds (0.226Kgrams)
Weight (shipping)	1.0 pounds (0.453Kgrams)
Mounting	Standard IBM PC/XT ½ slot
Safety Compliance	UL, CSA, FCC Class B

Section 2 INSTALLATION

2.1 Introduction

This section contains information on unpacking the drive, hardware preparation, installation and software availability.

2.2 Unpacking the Host Adapter

The host adapter is shipped in a carton and an electrostatic discharge (ESD) protective bag. Only after taking the proper precautions to prevent ESD damage may the adapter be removed from the protective bag.

WARNING The discharge of electrostatic energy that accumulates on the surface of the human body or other surfaces will damage or destroy the electronic components used in this device.

2.2.1 Electrostatic Discharge (ESD) Protection

Before removing the host adapter from its protective bag, prepare a static safe working area. The surface on which the adapter will be placed should be conductive. Conductive mats are available at most electronics supply dealers. A grounded conductive wrist strap should be worn at all times when handling the adapter. If a wrist strap is not available, insure that some part of your body remains in contact with a ground source (ie. the computer chassis if the line cord is connected) at all times while handling the drive. To reduce the possibility of ESD damage, handle the adapter by the edges or the mounting bracket. Even after the adapter is mounted in the computer chassis and properly grounded, ESD will still cause serious damage. Avoid touching any components or connectors on the adapter circuit board. Save the ESD bag and desiccant pack incase in the adapter needs to be repackaged.

2.2.2 Environmental and Shock Protection

The host adapter can be easily damaged by subjecting it to adverse temperature and humidity conditions as well as by mishandling. When packaged for shipment, a desiccant pack is enclosed in the ESD bag to absorb any unusually high amounts of moisture that may enter the bag. When the adapter has been stored in a cool, dry location and is moved to a warmer, more humid location for unpacking, the adapter should be allowed the temperature stabilize for at least 30 minutes before opening the ESD bag. If a cool adapter is exposed to warm. humid air, moisture will condense on the surface on the surface. Some components can be severely damaged by this moisture.

The way that the host adapter is handled can also affect the reliability. Even a small drop of 1 inch onto a hard surface can cause the adapter to become damaged. When handling the adapter on a work bench, a conductive rubber mat should be used. This will reduce the possibility of damage if the adapter is dropped.

2.3 Quick Start Configuration

This paragraph outlines the basic information needed to quickly configure the host adapter for use in most systems. For more detailed jumper configuration information, refer to section 2.4.

The tape drive included in your kit comes from the factory with the jumpers pre-set, no changes should be required. On the controller board, the DMA channel, Interrupt, and I/O Address must be checked to avoid conflicts with other hardware options. If you experience problems with operating the backup sys-

I/O Address Switch Settings

Address Bit	A1	A2	A3	A4	A5	A6	A7	A8	A9	
SW Position	1	2	3	4	5	6	7	8	9	10
Desired Address										
288H	On	On	Off	On	On	On	Off	On	Off	NA
2ACH	On	Off	Off	On	Off	On	Off	On	Off	NA
300H*	On	On	On	On	On	On	On	Off	Off	NA
338H	On	On	Off	Off	Off	On	On	Off	Off	NA

* Default Setting

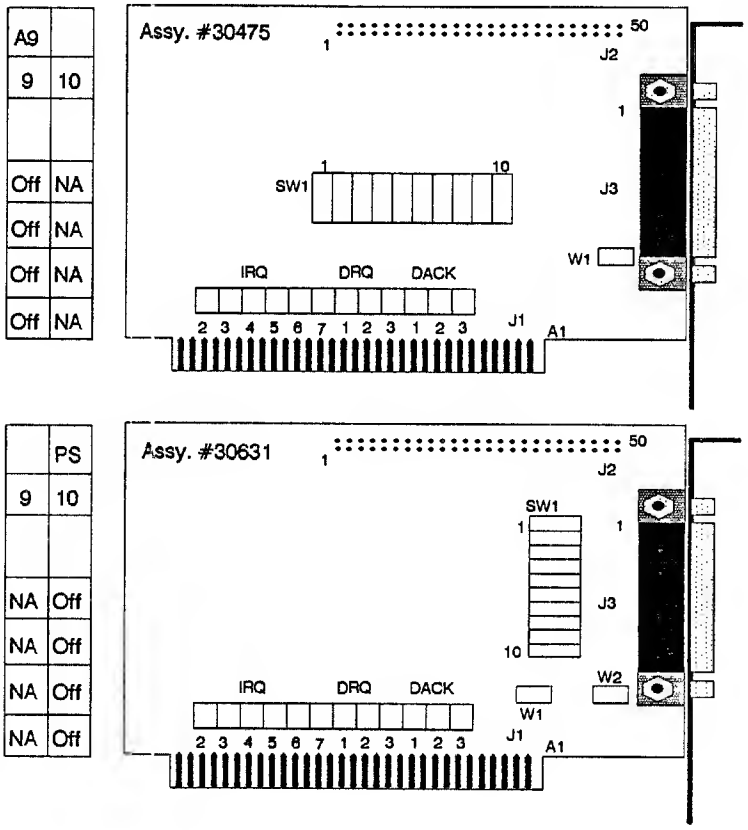


Figure 2-1
PC-02 Host Adapter Jumper and Switch Locations

Table 2-1
Default Jumper Settings

Assy. #30475					
Jumper	IN	OUT	Jumper	IN	OUT
W1	X		DRQ1	X	
IRQ2		X	DRQ2		X
IRQ3	X		DRQ3		X
IRQ4		X	DACK1	X	
IRQ5		X	DACK2		X
IRQ6		X	DACK3		X
IRQ7		X			

Assy. #30631					
Jumper	IN	OUT	Jumper	IN	OUT
W1	X		W2	X	
IRQ2		X	DRQ1	X	
IRQ3	X		DRQ2		X
IRQ4		X	DRQ3		X
IRQ5		X	DACK1	X	
IRQ6		X	DACK2		X
IRQ7		X	DACK3		X

tem using these quick start configurations, refer to section 2.6. Refer to Figure 2-1 for host adapter jumper and switch locations. Refer to Table 2-1 for the Default Jumper settings.

2.3.1 Quick Start Configuration - IBM AT Running PC-DOS/MS-DOS

The I/O address comes preset from the factory to 300H. The DMA will be set to DRQ=1 and DACK=1. The interrupt will be set to IRQ=3. These settings will work for most basic AT configurations.

2.3.2 Quick Start Configuration - IBM AT Running SCO Xenix or Interactive Unix

The I/O address for operation with SCO Xenix must be set to 338H. Set switches 1, 2, 6 & 7 to the ON or closed position and all other switches to the OFF or open position. The DMA must be set to DRQ=1 and DACK=1. The interrupt must be set to IRQ=5.

2.3.3 Quick Start Configuration - IBM AT Running The PICK Operating System

The I/O address for operation with PICK must be set to 338H. Set switches 1, 2, 6 & 7 to the ON or closed position and all other switches to the OFF or open position. The DMA must be set to DRQ=3 and DACK=3. The interrupt must be set to IRQ=5.

2.3.4 Quick Start Configuration - Novell Netware Operating System

The I/O address for operation with Novell Netware must be set to 338H. Set switches 1, 2, 6 & 7 to the ON or closed position and all other switches to the OFF or open position. The DMA must be set to DRQ=2 and DACK=2. The interrupt must be set to IRQ=6.

2.3.5 Quick Start Configuration - AT&T 6300 Running MS-DOS

The I/O address for operation in the AT&T 6300 must be set to 288H. Set switches 1, 2, 4, 5, 6 & 8 to the ON or closed position and all other switches to the OFF or open position. The DMA must be set to DRQ=1 and DACK=1. The interrupt must be set to IRQ=2.

2.4 Host Adapter Preparation - Assy. #30631

The host adapter contains several option jumpers that must be configured for proper operation before installation in the system unit. The locations of these jumpers can be found in Figure 2-1. The default jumper settings can also be found in Figure 2-1. The default configuration is for installation in the IBM AT. The jumper blocks consist of two rows of wire pins protruding up from the board about 3/8". Jumper connections are made by installing or moving one of the blue or black plastic jumper blocks between the proper pin pairs. Refer to Figure 2-2 for proper jumper installation. Extra jumpers may be removed from the drive or installed in a "not connected" position, as shown in Figure 2-2, for future use.

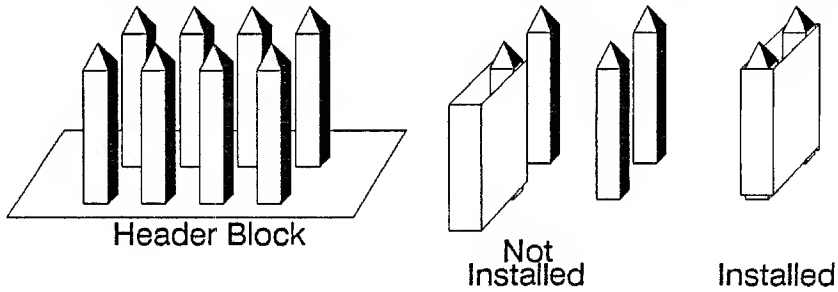


Figure 2-2
Option Jumper Installition

2.4.1 DRQ 1-3 & DACK 1-3 - DMA Channel Select

These jumpers select the desired DMA channel for the host adapter. The DRQ and DACK jumpers must be configured for the same channel (ie. if the DRQ1 jumper is installed, the DACK1 jumper must be installed). The default for this configuration is DRQ1 & DACK1 installed and all others not installed.

2.4.2 IRQ 2-7 - Interrupt Select

These jumpers configure the host adapters hardware interrupt priority, IRQ 2 has the highest priority and IRQ 7 the lowest. The selection of an interrupt must be chosen to avoid conflicts with other hardware options in your computer application. The default for this configuration is IRQ 3 installed and all others not installed.

2.4.3 SW1 Positions 1 thru 8 - I/O Address Select

These switches configure the input/output address for the host adapter. The value may range from 200H to 3FEH. The selection of an input/output address must be chosen to avoid conflicts with other hardware options in your computer. Refer to Figure 2-3 for proper switch setting. Refer to Figure 2-1 for the default and common address switch settings.

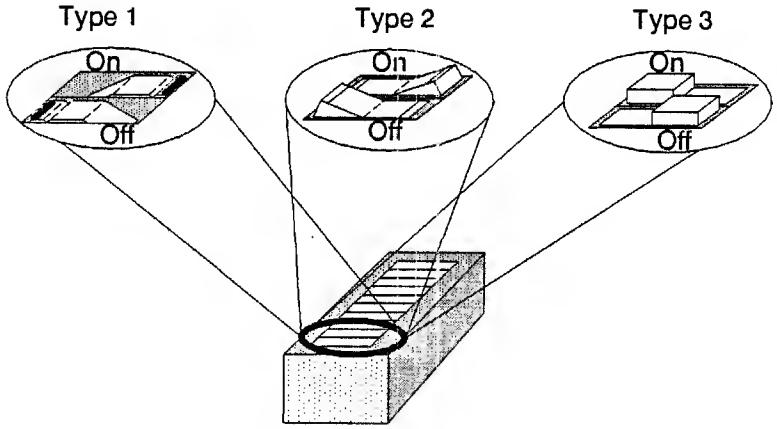


Figure 2-3
On/Off Switch Settings

2.4.4 W1 - DMA Inhibit

When this jumper is installed, DMA operation will be inhibited when an exception occurs. When not installed, DMA operations will continue if an exception occurs.

2.4.5 W2 - Ground Isolation

When this jumper is installed, the main board logic ground is connected to the chassis ground. When not installed, the main board logic ground is isolated from the chassis ground by a 0.1 microfarad capacitor. The default for this configuration is installed.

2.5 Host Adapter Preparation - Assy. #30475

The host adapter contains several option jumpers that must be configured for proper operation before installation in the system unit. The locations of these jumpers can be found in Figure 2-1. The default jumper settings can also be found in Figure 2-1. The default configuration is for installation in the IBM AT. The jumper blocks consist of two rows of wire pins protruding up from the board about 3/8". Jumper connections are made by installing or moving one of the blue or black plastic jumper blocks between the proper pin pairs. Refer to Figure 2-2 for proper jumper installation. Extra jumpers may be removed from the drive or installed in a "not connected" position, as shown in Figure 2-2, for future use.

2.5.1 DRQ 1-3 & DACK 1-3 - DMA Channel Select

These jumpers select the desired DMA channel for the host adapter. The DRQ and DACK jumpers must be configured for the same channel (ie. if the DRQ1 jumper is installed, the DACK1 jumper must be installed). The default for this configuration is DRQ1 & DACK1 installed and all others not installed.

2.5.2 IRQ 2-7 - Interrupt Select

These jumpers configure the host adapters hardware interrupt priority, IRQ 2 has the highest priority and IRQ 7 the lowest. The selection of an interrupt must be chosen to avoid conflicts with other hardware options in your computer application. The default for this configuration is IRQ 3 installed and all others not installed.

2.5.3 I/O Address Select

These switches configure the input/output address for the host adapter. The value may range from 000H to 3FEH. The selection of an input/output address must be chosen to avoid conflicts with other hardware options in your computer. Refer to Figure 2-3 for proper switch setting. Refer to Figure 2-1 for the default and common address switch settings.

2.5.4 W1 - Ground Isolation

When this jumper is installed, the main board logic ground is connected to the chassis ground. When not installed, the main board logic ground is isolated from the chassis ground by a 0.1 microfarad capacitor. The default for this configuration is installed.

2.6 Software Availability

The PC-02 tape backup system is compatible with the SY-TOS tape backup software manufactured by Sytron Corporation. It provides a user friendly, menu driven user interface to provide easy disk backup and restore operations. It is available in versions to operate under the PC-DOS/MS-DOS, Xenix and some Unix operating systems. For more information regarding the SY-TOS tape backup software and operation, refer to the SY-TOS Software Installation and Operation Manual provided with the software. For pricing and availability of the SY-TOS software, contact your local Wangtek distributor, Wangtek or Sytron Corporation.

2.7 If You Have A Problem During Installation

If the drive does not perform as described after installation, the following items should be checked before calling for assistance:

- Are all cable connectors seated properly?
- Is the data cartridge installed properly?
- Is the data cartridge write enabled?
- Is the software installed properly?
- Is the software configured properly?
- Are the computer option switches configured properly?
- Is the tape head clean?

If the problem persists, try to isolate the problem to the drive, computer, or software. Use the fault symptom guides that follow. If you need assistance isolating the fault, contact the dealer or distributor where you purchased the equipment. Do not return the drive to the dealer, distributor, or Wangtek without first contacting them to receive a return authorization. Drives returned to Wangtek without a Return Materials Authorization (RMA) number will be refused and returned to the sender at the sender's expense.

2.7.1 Drive Fault Symptoms

The following are symptoms of drive induced faults:

- If the tape drive select light flashes a repeating sequence of 2 or 3 short pulses followed by a 2-3 second pause.
- If the tape drive select light remains on at all times.
- If the tape drive does not perform the recalibration seek (fast tapping sound) when a cartridge is installed.

2.7.2 Host Adapter Fault Symptoms

The following are symptoms of host adapter board induced faults:

- If the computer system will not boot with the host adapter installed but boots correctly when removed.

2.7.3 Computer Fault Symptoms

The following are symptoms of computer induced faults:

- If the computer will not boot from the hard disk when the tape drive and controller are removed.

2.7.4 Software Fault Symptoms

The following are symptoms of software induced faults:

- If, when the software is run, the system hangs or locks up. Check the software configuration.
- If the software performs properly when first installed, but stops working sometime later. Reinstall the software from the original diskettes only.

Section 3 INTERFACE

3.1 Introduction

This section contains information about the PC-02 power connections, interface specifications and command usage. The Host Adapter is contained on a single board. Connectors are provided for the host and drive. The board is designed to mount in an expansion slot in an IBM PC, XT, AT, or a compatible.

3.2 PC-02 Power Requirements

The input power to the PC-02 is provided from the host computer bus through the J1 I/O connector. The voltages and current required to operate the Controller are shown in the following Table along with the applicable pin numbers of the J1 I/O connector.

Table 3-1
PC-02 Power Connections and Requirements

PIN NUMBER	PIN NAME	VOLTAGE MINIMUM	VOLTAGE MAXIMUM	CURRENT	COMMENTS
B1, B10, B31	GND	-----	-----	-----	Return (+5 VDC/+12 VDC) (See Note 1)
B3, B29	V5+	4.85	5.25	0.5A	+5 VDC (See Note 2)

Note 1: Must be tied together and to ground at one point in power supply.
Note 2: All voltages measured at J1 I/O connector.

3.3 Host Interface Signal Levels

All signals to the host are standard Tri-State TTL levels as follows:

False = High = 2.4 to 5.25 VDC
True = Low = 0 to 0.8 VDC
Off = High Impedance State

Voltages shall be measured at the Host Adapter Connector.

3.3.1 Signal Load

Signals from the Host to the PC-02 are loaded by not more than 2.0 ma. Command, Address, DMA and Interrupt request lines drive into not more than two LS245 inputs. The data lines drive into a single LS245 input.

3.4 Host Interface Signals

The host computer interface to the PC-02 is via the 62-pin card edge connector J1. The board utilizes one ½ length slot in the host. The I/O Channel is an extension of the PC microprocessor bus. It is however demultiplexed, repowered, and enhanced by the addition of interrupts and direct memory access (DMA) functions.

The I/O channel contains an 8-bit, bi-directional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channel of DMA control lines, memory

refresh timing control lines, a channel-check line, and power and ground for the adapters. Four voltage levels are provided for I/O cards: +5 VDC, -5 VDC, +12 VDC, and -12 VDC. These functions are provided in a 62-pin connector with 100-mil card tab spacing. For additional information refer to IBM PC Technical Reference Manual.

The following paragraphs provide a description of the IBM Personal Computer XT I/O Channel. All lines are TTL-compatible. Signal pinouts are shown in Table 3-2. IBM PC I /O channel signal orientation is shown in Figure 3-1. The reference in parenthesis next to each signal mnemonic indicates the signal direction (I = Input, O = Output or I/O = Bi-directional) in reference to the host. Those mnemonics noted with an astrisk (*) are low active.

3.4.1 OSC (O)

OSCILLATOR: High-speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.

3.4.2 CLK (O)

SYSTEM CLOCK: It is a divide-by-three of the oscillator and has a period of 2.0 ns (4.77 MHz). The clock has a 33% duty cycle.

3.4.3 RESET DRIVE (O)

This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.

3.4.4 A0 - A19 (O)

ADDRESS BITS 0 TO 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 Megabyte of memory. A0 is the Least Significant Bit (LSB) and A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.

3.4.5 D0 - D7 (I/O)

DATA BITS 0 - 7: These lines provide data bus bits 0 to 7 for the processor, memory and I/O devices. D0 is the Least Significant Bit (LSB). These lines are active high.

3.4.6 ALE (O)

ADDRESS LATCH ENABLE: This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a valid processor address (when used with AEN). Processor addresses are latched with the failing edge of ALE.

3.4.7 I/O CHB CK* (I)

-I/O CHANNEL CHECK: This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error is indicated.

3.4.8 I/O CH RDY (I)

I/O CHANNEL READY: This line, normally high (Ready), is pulled low (Not Ready) by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This line should never be held low longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles (210 ns).

3.4.9 IRQ2 - IRQ7 (I)

INTERRUPT REQUEST 2 - 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor (Interrupt Service Routine).

3.4.10 IOR* (O)

-I/O READ COMMAND: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

3.4.11 IOW* (O)

-I/O WRITE COMMAND: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

3.4.12 MEMW* (O)

MEMORY WRITE COMMAND: This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

3.4.13 DRQ1 - DRQ3 (O)

DMA REQUEST 1 - 3: These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK lines goes active.

3.4.14 DACK0*-DACK3* (O)

-DMA ACKNOWLEDGE 0 - 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active low.

Table 3-2
J1 Host Interface Pin Assignments

J1 PIN NO.	NAME	SIGNAL DESCRIPTION
A1	I/O CH CK*	I/O Channel Check
A2	D7	
A3	D6	
A4	D5	
A5	D4	Data Bits 0 - 7
A6	D3	D0 = LSB
A7	D2	D7 = MSB
A8	D1	
A9	D0	
A10	I/O CH RDY	I/O Channel Ready
A11	AEN	Address Enable
A12	A19	
A13	A18	
A14	A17	
A15	A16	
A16	A15	
A17	A14	
A18	A13	
A19	A12	Address Bits 0 - 19
A20	A11	
A21	A10	A0 = LSB
A22	A9	A19 = MSB
A23	A8	
A24	A7	
A25	A6	
A26	A5	
A27	A4	
A28	A3	
A29	A2	
A30	A1	
A31	A0	

J1 PIN NO.	NAME	SIGNAL DESCRIPTION
B1	GND	Ground
B2	RESET DRIVE	Reset or Initialize
B3	+5 VDC	
B4	IRQ2	Interrupt Request #2
B5	-5 VDC	
B6	DRQ2	DMA Request #2
B7	-12 VDC	
B8	CARD SELECT*	Card Selected
B9	+12 VDC	
B10	GND	Ground
B11	MEMW*	Memory Write Command
B12	MEMR*	Memory Read Command
B13	IOW*	I/O Write Command
B14	IOR*	I/O Read Command
B15	DACK3*	DMA Acknowledge #3
B16	DRQ3	DMA Request #3
B17	DACK1*	DMA Acknowledge #1
B18	DRQ1	DMA Request #1
B19	DACK0*	DMA Acknowledge #0
B20	CLOCK	System Clock
B21	IRQ7	
B22	IRQ6	
B23	IRQ5	Interrupt Request 3 - 7
B24	IRQ4	
B25	IRQ3	
B26	DACK2*	DMA Acknowledge #2
B27	T/C	Terminal Count
B28	ALE	Address Latch Enable
B29	+5 VDC	
B30	OSC	Oscillator = Hi Speed Clock
B31	GND	Ground

NOTE: * = Negative True

3.4.15 AEN (O)

ADDRESS ENABLE: This line is used to de-gate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control of the address bus, data bus, read command lines (memory and I/O), and the write command lines (Memory and I/O).

3.4.16 T/C (O)

TERMINAL COUNT: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

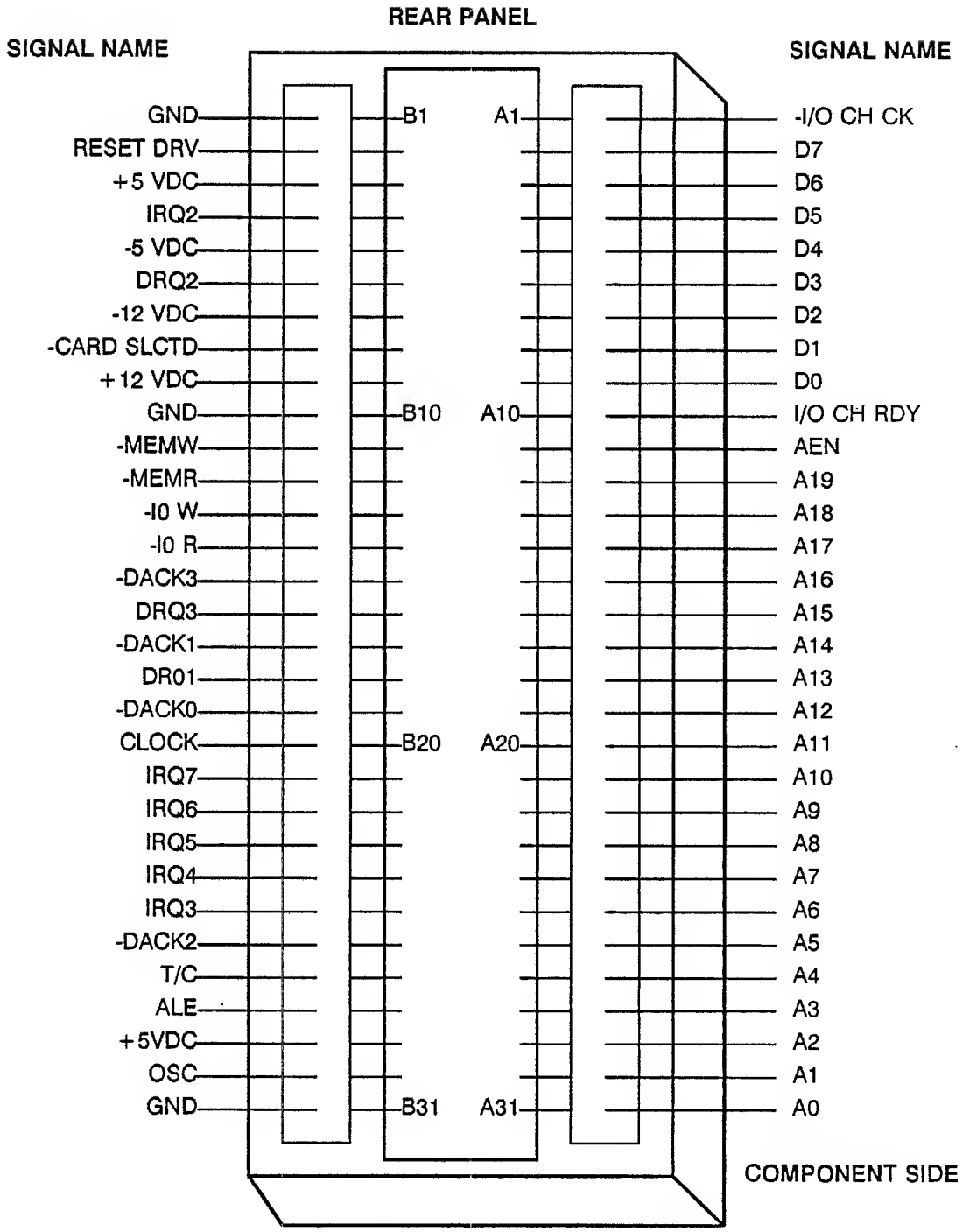


Figure 3-1
IBM PC/XT I/O Channel Signal Orientation

3.4.17 CARD SLCTD* (I)

-CARD SELECTED: This line is activated by cards in expansion slot J8. It signals the system board that the card has been selected and that appropriate drivers on the system board should be directed to either read from, or write to, expansion slot J8. Connectors J1 through J8 are tied together at this pin, but the system board does not use their signal. This line should be driven by an open collector device.

The following voltages are available on the system board I/O channel:

+5 VDC ±5% on 2 connector pins (B3, B29)
-5 VDC ±10% on 1 connector pin (B5)
+12 VDC ±5% on 1 connector pin (B9)
-12 VDC ±10% on 1 connector pin (B7)
GND (Ground), located on 3 connector pins (B1, B10, B31)

3.5 Host I / O Port Interface

Interfacing to the PC-02 Host Adapter board is accomplished by addressing two default ports as shown in Table 3-3:

Table 3-3
Host I/O Ports

NAME	ADDRESS (HEX)	READ / WRITE FUNCTION
STATUS PORT	BASE	READ ONLY
CONTROL PORT	BASE	WRITE ONLY
COMMAND PORT	BASE +1	WRITE ONLY
DATA PORT	BASE +1	READ / WRITE

3.5.1 Status Port

Reading from the selected I/O port address shall input the following QIC-02 operational status as defined by the QIC-02 specification to the computer.

The adapter generates an Interrupt (if enabled) when status bits 0 or 1 become active low.

Table 3-4
Status Port Bit Definations

Bit	Signal
0	$\overline{\text{Ready}}$
1	$\overline{\text{Exception}}$
2	$\overline{\text{Direction}}$
3	Reserved
4-7	Not Used

3.5.2 Control Port

Writing to the selected I/O port address sends the following control directives to the device.

Table 3-5
Control Port Bit Definations

Bit	Signal
0	Online
1	Reset
2	Request
3	Enable DMA (1 or 2) and Interrupt
4	Enable DMA (3) and Interrupt
5-7	Not Used

3.5.3 Command Port

Writing to the selected I/O port address plus 1 transfers the standard QIC-02 commands, as defined by the QIC-02 specification, to the device.

3.5.4 Data Port

Writing to or Reading from the selected I/O port address plus 1 shall transfer data between the host computer and the device. Reading from the selected I/O port address plus 1 shall also input the six (6) status byte descriptions of the device to the host computer.

3.6 Drive Interface Connector

The PC-02 interfaces with a tape drive via J2 (for internal configurations) or J3 (for external configurations) using the QIC-02 interface standard. The J2 signal connector on the board is a fifty conductor plug connector. The recommended connector is a AMP 88379-8 or equivalent. The signal cable shall be a fifty conductor, flat ribbon cable. This interface supports a total cable length of three meters or ten feet maximum using a cable of 100 ohms characteristic impedance $\pm$10%. The interface signal connector pin assignments for J2 are listed in Table 3-6. The J3 external signal connector is a DB-37 plug connector. The signal cable shall be a 37 conductor cable. This interface supports a total cable length of three meters or ten feet maximum using a cable of 100 ohms characteristic impedance $\pm$10%. The interface signal connector pin assignments for J3 are listed in Table 3-7. All PC-02/drive interface signals must be terminated by 220 ohms to +5 VDC and 330 ohms to ground. Refer to Figure 3-2. Data and commands are transferred to and from the drive on an eight bit bi-directional data bus using asynchronous handshaking techniques to eliminate rigorous timing constraints.

3.6.1 Drive Interface Signal Levels

All signals to the drive are standard Tri-State TTL levels as follows:

False, (Logic 0) = High = 2.4 to 5.25 VDC
True, (Logic 1) = Low = 0.0 to 0.55 VDC
Off = High Impedance State

Voltages should be measured at the PC-02 connector J2.

3.6.2 Drive Signal Loading

Signals from the PC-02 to the drive should be loaded on the interface by no more than 2.0 mA plus the required terminations. Data bus signals use a bi-directional tranceiver as shown in Figure 3.2. Control signals use a uni-directional tranceiver configuration as shown in Figure 3-2. Signals from the drive to the PC-02 are loaded on the interface by no more than 2.0 mA plus the required terminations.

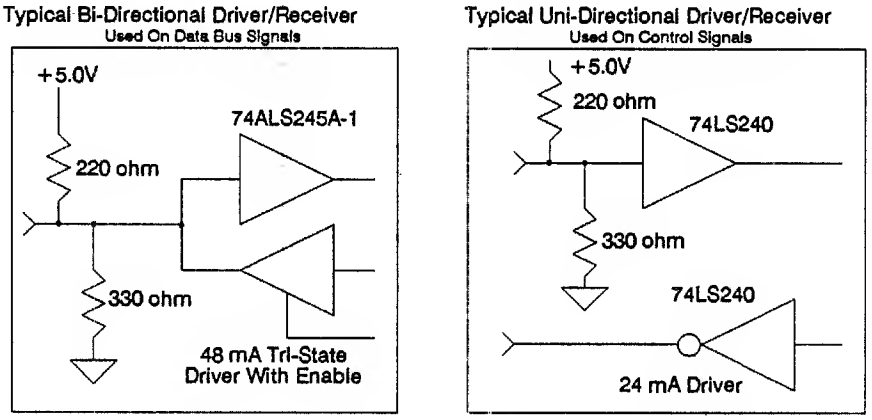


Figure 3-2
Interface Signal Terminations

Table 3-6
J2 Interface Connerctor Pin Assignments

Pin#	Mnemonic	To	Description
02-10			Reserved for future use.
12	HB7-	B	Host Bus Bit #7, MSB
14	HB6-	B	Host Bus Bit #6
16	HB5-	B	Host Bus Bit #5
18	HB4-	B	Host Bus Bit #4
20	HB3-	B	Host Bus Bit #3
22	HB2-	B	Host Bus Bit #2
24	HB1-	B	Host Bus Bit #1
26	HB0-	B	Host Bus Bit #0, LSB
28	ONL-	D	Online
30	REQ-	D	Request
32	RSTC-	D	Reset Controller
34	XFR-	D	Transfer
36	ACK-	H	Acknowledge
38	RDY-	H	Ready
40	EXC-	H	Exception
42	DIR-	H	Direction
44-50			Reserved for future use.

NOTE: All odd pins are signal returns, which should be connected to ground at both the drive and the host. B = Bi-directional, D = Drive, H = Host.

Table 3-7
J3 Interface Connerctor Pin Assignments

Pin#	Mnemonlc	To	Description
1	PWS	D	Power On Sense
2	HB7-	B	Host Bus Bit #7, MSB
3	HB6-	B	Host Bus Bit #6
4	HB5-	B	Host Bus Bit #5
5	HB4-	B	Host Bus Bit #4
6	HB3-	B	Host Bus Blt #3
7	HB2-	B	Host Bus Bit #2
9	HB1-	B	Host Bus Blt #1
9	HB0-	B	Host Bus Bit #0, LSB
10	ONL-	D	Online
11	REQ-	D	Request
12	RSTC-	D	Reset Controller
13	XFR-	D	Transfer
14	ACK-	H	Acknowledge
15	RDY-	H	Ready
16	EXC-	H	Exceptlon
17	DIR-	H	Directlon
19			Reserved for future use.
18, 20-37			Ground
NOTE: B = Bi-directional, D = Drive, H = Host.			

3.6.3 Online (ONL)

This signal is generated by the host and is true when the drive is either writlng, reading or searching. In all other operations, the state of this slgnal Is not relevant. Deasserting the ONLINE signal terminates a write or read operatlon and rewlnds the tape to BOT. During deselection and selection of the drive, while at position, care must be taken to avold unwanted rewlnds as a result of the ONLINE signal. Following a write or read operatlon, the drlve does not perform rewlnd when deselected with ONLINE asserted. When re-selected the drive will sample the state of ONLINE. A rewind does not occur if selection is made with ONLINE asserted or deasserted. However, the host must assert ONLINE prlor to any subsequent read or write operations.

3.6.4 Request (REQ)

This signal is generated by the host to initiate and execute command transfers. REQUEST is also used to handshake with READY when transferring status information from the drive to the host. This signal should be asserted only when an EXCEPTION or READY is asserted.

3.6.5 Reset (RSTC)

This signal is generated by the host. The drive Is reset and operating parameters are initialized. After RESET, the drive will assert EXCEPTION.

3.6.6 Transfer (XFR)

This signal is generated by the host to indicate that data is being placed on the data bus in write mode or that data has been taken from the bus in read mode. TRANSFER is used in conjunction with ACKNOWLEDGE to move data between the drive and host.

3.6.7 Acknowledge (ACK)

This signal is generated by the drive to indicate that data has been accepted from the data bus in write mode or that data is being placed on the bus in read mode. ACKNOWLEDGE is used in conjunction with TRANSFER to move data between the drive and host.

3.6.8 Ready (RDY)

This signal is generated by the drive to indicate one of the following conditions:

- The drive is available to receive and execute a new command.
- A new block is ready for transfer during a read operation.
- The drive is ready to receive a new block during write operation.

The drive is ready to transfer status information to the host when REQUEST is asserted.

3.6.9 Exception (EXC)

This signal is generated by the drive to indicate that it has information for the host. After a RESET, EXCEPTION is always asserted. EXCEPTION may be asserted during an operation and should be treated with priority. After EXCEPTION, the only legal command that shall be transmitted to the drive is Read Status.

3.6.10 Direction (DIR)

This signal is generated by the drive to indicate the direction of the bus. The asserted state of DIRECTION indicates that transfers are from the drive to the host.

3.6.11 Power On Sense (PWS)

This signal is used to inform an external drive subsystem when the host power is on. The function of the signal is controlled by SW1 switch 10 **(Assy.#30631 only).**

3.7 Drive Commands

The PC-02 communicates with the drive via the QIC-02 Intelligent Drive interface. The QIC-02 standard and optional commands are provided in Table 3-8 for reference only.

Table 3-8
QIC-02 Standard & Optional Command Sets

Command	Op Code Bits 7654 3210	Hex Value	Standard or Optional
Select Drive	0000 0001	01	S
Select QIC-24 Format	0010 0111	27	S
Select QIC-120 Format	0010 1000	28	S
Select QIC-150 Format	0010 1001	29	S
Write Data	0100 0000	40	S
Write Without Underruns	0100 0001	41	O
Write File Mark	0110 0000	60	S
Write File Mark / Write	0110 0010	62	O
Write File Mark / Write w/o Underruns	0110 0011	63	O
Read Data	1000 0000	80	S
Read Continuous	1000 0010	82	O
Read Block N	1000 1010	8A	O
Space Forward	1000 0001	81	O
Space Reverse	1000 1001	89	O
Search To End Of Recorded Media	1010 0011	A3	O
Read File Mark	1010 0000	A0	S
Read N Filemarks	1011 NNNN	B1-BF	O
Read Status	1100 0000	C0	S
Erase Tape	0010 0010	22	S
Initialize (retension) Tape	0010 0100	24	S
Rewind to BOT	0010 0001	21	S

NNNN = Value can range from 0001 to 1111.

Section 4 PARTS LISTS, APPENDIX AND SCHEMATICS

4.1 Introduction

This section contains the illustrated parts breakdown, recommended spare parts list, appendix, and schematics.

4.2 Illustrated Parts Breakdown

Figure 4-1 used in conjunction with Table 4-1 are used to identify and cross reference Wangtek part numbers for all replaceable subassemblies.

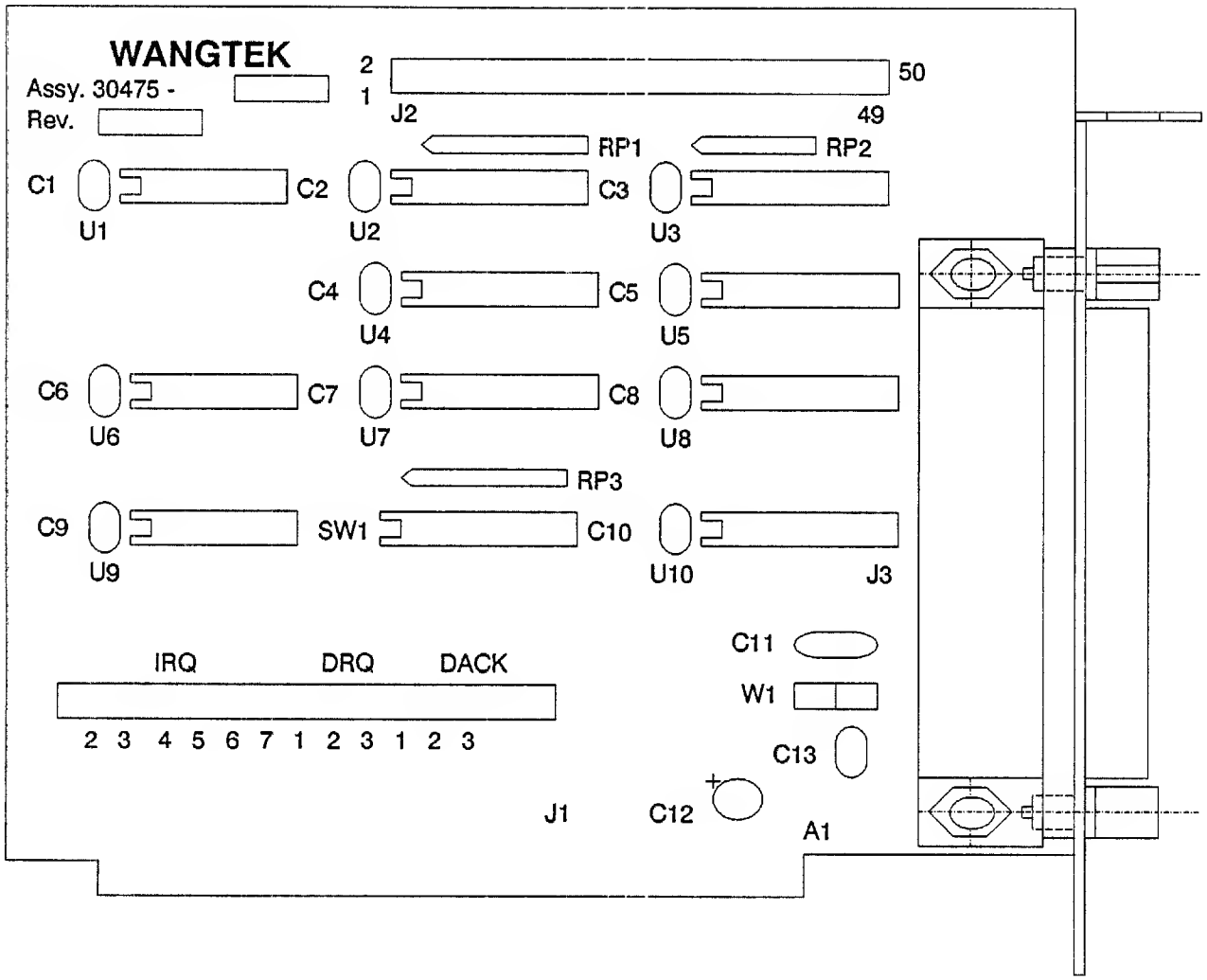


Figure 4-1
Illustrated Parts Breakdown - Assembly #30475-XXX

Table 4-1
Illustrated Parts List - Assembly #30475-XXX

ITEM	DESCRIPTION	PART NUMBER	QTY.	REMARKS
3	Header, 2 Pin, Double Row	55203-001	1	W1
4	Header, 24 Pin, Double Row	55203-024	1	IRQ2-7, DRQ1-3, DACK 1-3
5	Header, 50 Pin, Double Row	55203-050	1	J2 - PIN 35 REMOVED
6	Jumper, .100 In centers	55045-001	REF	
7	Socket, Dip, 20 Pin	50008-010	3	U6, 7, 9
9	IC, 74LS00	50019-001	1	U1
10	IC, 74LS374	50034-001	1	U3
11	IC, 74LS640	55383-001	1	U5
12	IC, 74LS240	50030-001	1	U4
13	IC, 74LS244	50031-001	1	U8
14	IC, 74LS174	55171-001	1	U10
15	IC, 74LS245	55188-001	1	U2
16	IC, PAL Programmed	55187-003	1	U7
17	IC, PAL Programmed	55191-003	1	U6
18	IC, PAL Programmed	55191-001	1	U9
20	Switch, Dip 10 Positions	55202-001	1	SW1
22	Capacitor, Tant, R/L, 20V 10% 4.7 UF	55242-475	1	C12
23	Capacitor, 50V ±20% .1 MF	55246-001	12	C1 - 11, C13
25	Resistor, Pack 220/330 Ohms	55247-001	1	RP1
26	Resistor, Sip - 6 Pin 220/330	55225-001	1	RP2
27	Resistor, Sip - 10 Pin 4.7K Ohms	50015-472	1	RP3
28	Bracket, Mounting PC-36	21015-001	1	
33	Receptacle Assembly, R/A 37 Cont.	55384-008	1	J3
36	Screw, P/H CR 4-40 X 3/8"	55137-206	2	
37	Washer, Flat, Nylon	55209-001	2	
38	Nut, Hex 4-40	55104-200	2	
39	Washer, Split Lock #4	55109-200	2	
40	Standoff, ML, FML, Threaded	55342-001	2	

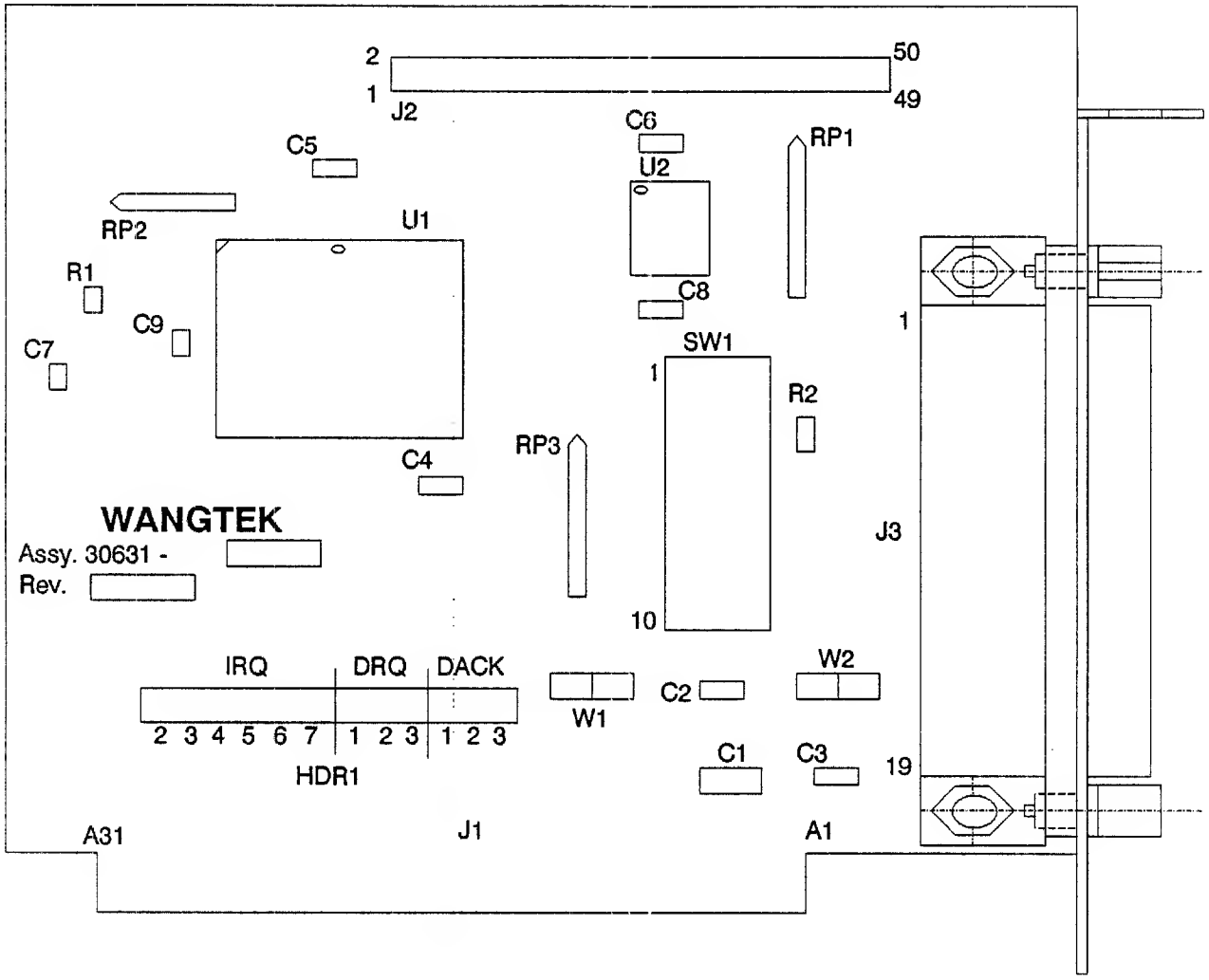


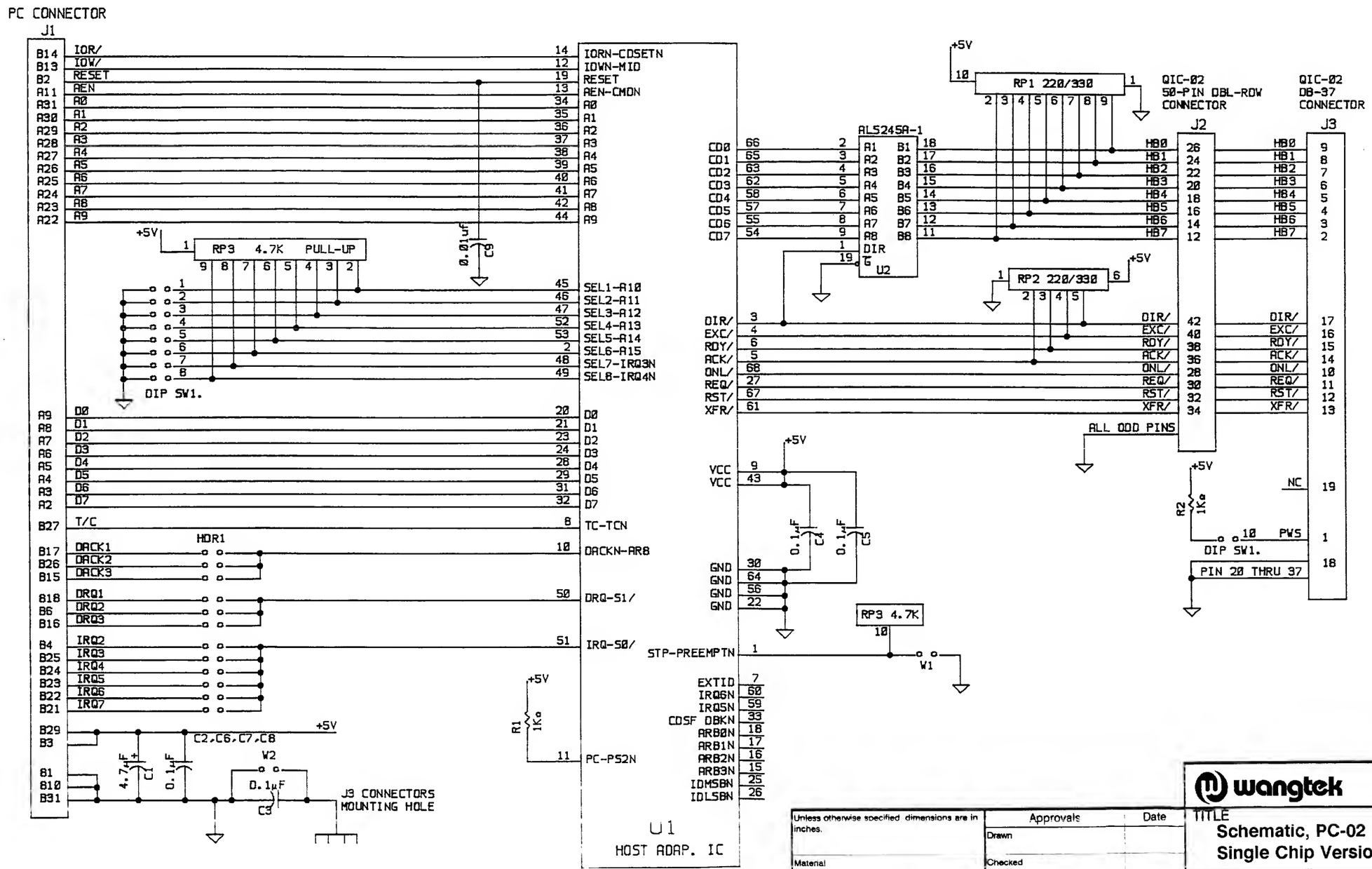
Figure 4-2
Illustrated Parts Breakdown - Assembly #30631-XXX

Table 4-2
Illustrated Parts List - Assembly #30631-XXX

ITEM	DESCRIPTION	PART NUMBER	QTY.	REMARKS
4	Header, 2 Pin, Double Row	55203-002	2	W1, W2
5	Header, 24 Pin, Double Row	55203-024	1	HDR1
6	Header, 50 Pin, R/A Double Row	55480-050	1	J2 - PIN 35 REMOVED
7	Jumper, .100 In centers	55045-001	REF	
9	IC, PC-PS2 Host Adapter, S/MNT	21337-001	1	U1
10	IC, 74ALS245A-1DW, S/MNT	55467-001	1	U2
11	Switch, Dip 10 Positions	55202-001	1	SW1
13	Resistor, Chip 1/8W 5% 1K Ohms	55479-102	2	R1, R2
14	Resistor, Sip - 10 Pin 4.7K Ohms	50015-472	1	RP3
15	Resistor, Sip - 10 Pin 220/330 Ohms	55247-001	1	RP1
16	Resistor, Sip - 6 Pin 220/330 Ohms	55225-001	1	RP2
17	Capacitor, Chip, Cer, 5% 0.01μF	55477-103	1	C9
18	Capacitor, Chip, Tant, 4.7μF	55482-475	1	C1
19	Capacitor, Chip, Cer, 20% 0.1μF	55537-104	1	C2 - C8
21	Receptacle Assembly, R/A DB-37	55384-008	1	J3
24	Bracket, Mounting PC	21015-001	1	
27	Screw, P/H CR 4-40 X 3/8"	55137-206	2	
28	Washer, Flat, Nylon	55209-001	2	
29	Nut, Hex 4-40	55104-200	2	
30	Washer, Split Lock #4	55109-200	2	
31	Standoff, ML, FML, Threaded	55342-001	2	

4.3 Appendix A - Schematics

Application		Revisions			
Next Assy	Used On	Rev.	Description	Date	Approved
30631-XXX	PC-02 Host Adapter	A	Engineering Rel Per E.O.#		



Notes: Unless Otherwise Specified.

Unless otherwise specified dimensions are in inches.	Approvals	Date
Material	Drawn	
	Checked	
Finish	Issued	
DO NOT SCALE DRAWING Form WXXXA 2/89		

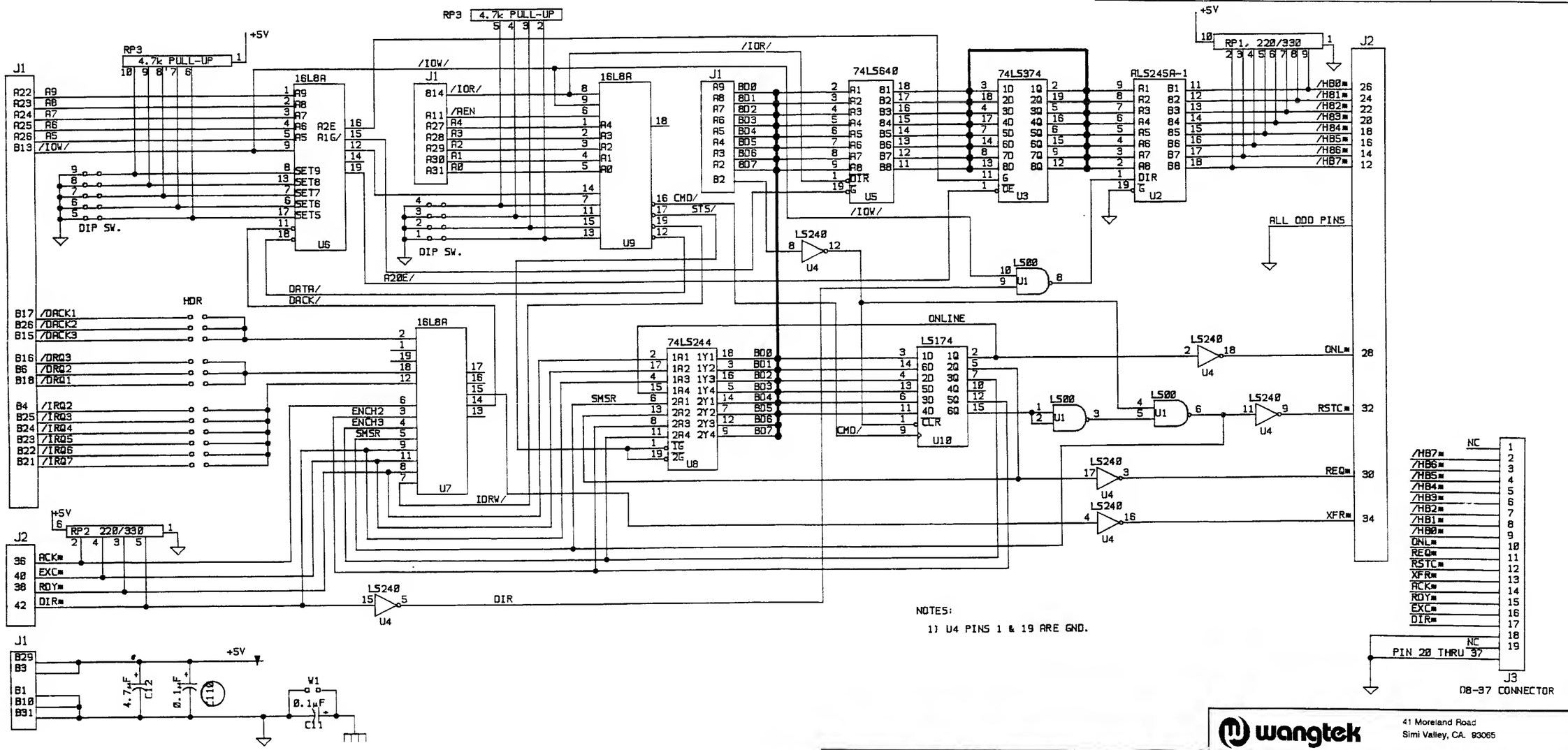
wangtek
41 Moreland Road
Simi Valley, CA. 93065

TITLE
Schematic, PC-02 Host Adapter
Single Chip Version

Size	FSCM	DWG. NO.	REV.
B		40832-001	A
Scale		Sheet 1 of 1	

Application	
Next Assy	Used On
30475-XXX	PC-02 Host Adapter

Revisions			
Rev.	Description	Date	Approved
A	Eng. Release Per E.O. #10792	11/13/87	
B	E.O. #11027	3/26/88	
C	E.O. #11585	8/22/88	



NOTES:

1) U4 PINS 1 & 19 ARE GND.

Notes: Unless Otherwise Specified.

Unless otherwise specified, dimensions are in inches.	Approvals		Date
	Drawn	G. Stroh	10/28/87
Material	Checked	S. Taheri	11/13/87
Finish	Issued	S. Taheri	11/13/87
DO NOT SCALE DRAWING			

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41 Moreland Road
Simi Valley, CA. 93065

TITLE: Schematic, PC-02 Host Adapter

Size	FSCM	DWG. NO.	REV.
B		40197-001	C

Scale | Sheet 1 of 1